(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 126 618 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
22.08.2001 Bulletin 2001/34

(51) Int Cl.[7]: **H03L 7/099**, H03K 5/156

(21) Application number: **01103754.6**

(22) Date of filing: **15.02.2001**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **17.02.2000 JP 2000039510**

(71) Applicant: **MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.**
Kadoma-shi, Osaka-fu 571 (JP)

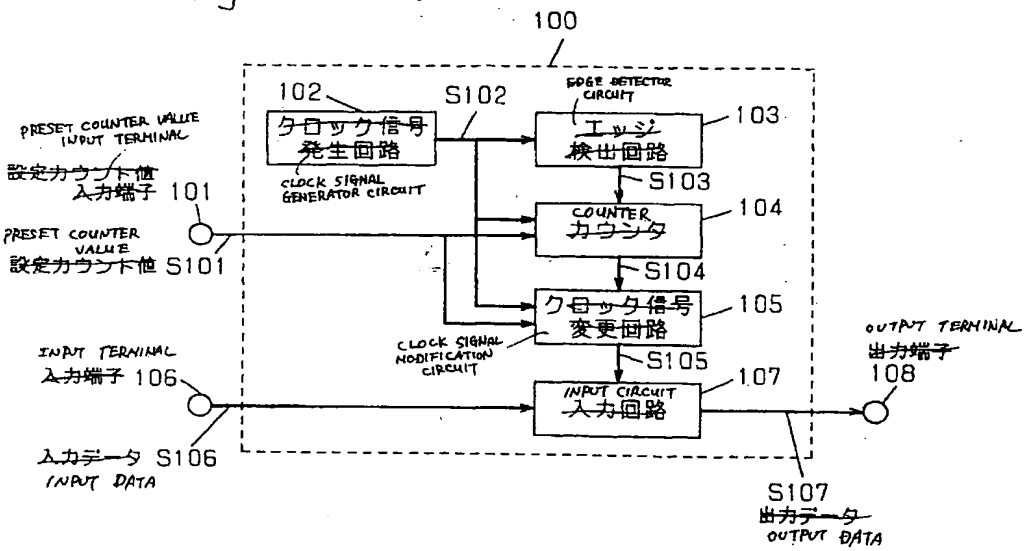
(72) Inventors:
- **Nishio, Takatoshi**
  Hirakata-shi, Osaka (JP)
- **Tabira, Yoshihiro**
  Osaka-shi, Osaka (JP)
- **Kau, Stefan,**
  55411 Bingen (DE)
- **Kiefner, Marcus**
  64297 Darmstadt (DE)

(74) Representative: **Grünecker, Kinkeldey,**
Stockmair & Schwanhäusser Anwaltssozietät
Maximilianstrasse 58
80538 München (DE)

(54) Clock signal generator and communication device using the same

(57) An edge detector circuit 103 detects the edge of an original clock signal S102 generated by the clock signal generator circuit 102. A counter 104 counts the number of edges of the original clock signal S102. The counter 104 is reset when the preset counter value S101 is reached, and repeats counting operation. A clock signal modification circuit 105 masks the original clock signal S102 when the counter value has reached the preset counter value to generate a baud rate control clock signal S105. An input circuit 107 latches input data S106 per predetermined rising edge of the clock signal with the band rate control clock signal S105 and outputs an output signal S107.

Fig. 1



EP 1 126 618 A2

Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a clock signal generator for generating a desired clock signal by adding a peripheral circuit to clock signal generating means and communications apparatus using the clock signal generator.

[0002] Asynchronous communications such as RS-232C are widely known and used in a variety of fields. Asynchronous communications are an essential feature for personal computers. A precise clock signal is required also in asynchronous communications. A variety of clock signal generators have been developed and added to a library.

[0003] In case asynchronous communications are carried out by using a conventional clock signal generator that has been added to a library, a desired clock signal thus a correct baud rate may not be obtained by frequency division. For example, according to the RS-232C specifications (EIA/TIA-22-E), a maximum transfer rate is 20 kbps although the transfer rate exceeds this limit in practice. This may cause problems such as a communication error thus requesting re-design of the entire communications apparatus.

[0004] While re-designing a clock signal generator can customize the frequency division feature of the clock signal and a precise baud rate can be obtained, a considerable increase in the number of development man-hours and another trouble may be caused by a new design.

SUMMARY OF THE INVENTION

[0005] The invention, in view of the aforementioned problems, aims at reducing the number of man-hours required for custom design of a clock signal generator, by having a configuration where an additional circuit is incorporated into an existing highly reliable clock signal generator circuit and an intermittent clock signal is generated to obtain a baud rate, instead of making a design by customizing a clock signal generator circuit for generating a clock signal whose frequency is constant.

[0006] In order to solve the aforementioned problems, a clock signal generator according to the first aspect of the invention comprises: clock signal generating means for generating a first clock signal, counting means for counting the number of clocks of the first clock signal, and masking means for generating a second clock signal by masking the first clock signal in case the counting means has reached a preset value.

[0007] In order to solve the aforementioned problems, a clock signal generator according to the second aspect of the invention is a clock signal generator according to the first aspect of the invention, characterized in that the counting means is periodically reset and that the masking means has a plurality of values as preset values.

[0008] In order to solve the aforementioned problems, a clock signal generator circuit according to the third aspect of the invention comprises: a clock signal generating means for generating a first clock signal and a modulation means for generating a second clock signal by modulating the first clock signal.

[0009] In order to solve the aforementioned problems, communications apparatus according to the fourth aspect of the invention uses a clock signal generator comprising: clock signal generating means for generating a first clock signal, counting means for counting the number of clocks of the first clock signal, and masking means for generating a second clock signal by masking the first clock signal in case the counting means has reached a preset value, to perform data input/output via the second clock signal generated by the clock signal generator.

[0010] In order to solve the aforementioned problems, communications apparatus according to the fifth aspect of the invention is communications apparatus according to the fourth aspect of the invention, characterized in that the counting means is periodically reset and that the masking means has a plurality of values as preset values.

[0011] In order to solve the aforementioned problems, communications apparatus according to the sixth aspect of the invention uses a clock signal generator comprising: a clock signal generating means for generating a first clock signal and a modulation means for generating a second clock signal by modulating the first clock signal, to perform data input/output via the second clock signal generated by the clock signal generator.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Fig. 1 is a block diagram of communications apparatus according to embodiment 1 of the invention.

[0013] Fig. 2 is a first timing chart explaining the operation of the communications apparatus shown in Fig. 1.

[0014] Fig. 3 is a second timing chart explaining the operation of the communications apparatus shown in Fig. 1.

[0015] Fig. 4 is a third timing chart explaining the operation of the communications apparatus shown in Fig. 1.

[0016] Fig. 5 is a block diagram of communications apparatus according to embodiment 2 of the invention.

[0017] Fig. 6 is a timing chart explaining the operation of the communications apparatus shown in Fig. 5.

[0018] Fig. 7 is a block diagram of communications apparatus according to embodiment 3 of the invention.

[0019] Fig. 8 is a timing chart explaining the operation of the communications apparatus shown-in Fig. 7.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0020] Embodiments of the invention will be described referring to the drawings.

(Embodiment 1)

[0021] A clock signal generator and communications apparatus using the clock signal generator according to embodiment 1 regenerates a baud rate clock signal by correcting a clock output by an existing clock generator circuit in generating a clock signal. Thus, the number of man-hours required for custom design of a clock signal generator is reduced in designing communications apparatus.

[0022] A clock signal generator and communications apparatus using the clock signal generator according to embodiment 1 will be described referring to Figs. 1 through 4.

[0023] Fig. 1 is a block diagram of a clock signal generator and communications apparatus using the clock signal generator according to embodiment 1 of the invention. The communications apparatus 100 is composed of a preset counter value input terminal 101, a clock signal generator circuit 102, an edge detector circuit 103, a counter 104. a clock signal modification circuit 105, an input terminal 106, an input circuit 107, and an output terminal 108.

[0024] Operation of the clock signal generator and the communications apparatus using the clock signal generator will be described. As shown in Fig. 2, the edge detector circuit 103, on detecting the rising edge of an original clock signal S102 generated by the clock signal generator circuit 102, outputs a High signal as an edge signal to the counter 104. The counter 104 is incremented when an edge signal S103 is input. The counter 104 is zero-cleared when the counter value S104 becomes identical with the preset counter value S101. The clock signal modification circuit 105 masks the original clock signal S102 in case the counter value S104 is identical with the preset counter value S101. Otherwise, the clock signal modification circuit 105 outputs a baud rate control clock signal S105 to the input circuit 107 without masking the original clock signal S102 . With the timing shown in Fig. 3, the input circuit 107 latches input data S106 per predetermined rising edge of the baud rate control clock signal S105 and sequentially outputs the input data S106 to an external data output terminal 108.

[0025] In this embodiment, a baud rate is realized via accuracy of the baud rate clock signal alone by generating an intermittent baud rate clock signal, instead of using a 4/3-times clock signal. Fig. 4 is a timing chart comparing the case where the input signal S106 is captured via a precision clock signal S400 (S401) and the case where the input signal S106 is captured via a baud rate control clock signal S105 (107) in case the precision clock signal S400 as a 4/3-times clock signal is generated with a clock signal generator circuit customized. As understood from comparison between S107 and S401, capture timing completely matches at 12 cycles for the output baud rate control clock signal and the precision clock signal. This eliminates the effects of capturing jitter caused by an intermittent signal.

[0026] As mentioned earlier, a desired baud rate is realized by performing communications via a baud rate clock signal regenerated using an intermittent clock signal even when conventional communications apparatus whose baud rate clock signal is less accurate. Such a configuration uses only a circuit that generates an intermittent clock signal for compensation. Thus the number of man-hours required for designing a customized clock signal generator circuit is drastically reduced.

[0027] While data input from the baud rate clock signal is specified as shown in Figs. 3 and 4, this invention is not limited to this configuration. While the clock signal modification circuit processes a delayed input baud rate control clock signal, the delay amount is variable and it is possible to process an input baud rate control clock signal without delay.

(Embodiment 2)

[0028] A clock signal generator and communications apparatus using the clock signal generator according to embodiment 2 of the invention is characterized in that the frequency range where a baud rate clock signal can be corrected is extended without substantially enhancing the circuit scale.

[0029] A clock signal generator and communications apparatus using the clock signal generator according to embodiment 2 will be described referring to Figs. 5 and 6.

[0030] Fig. 5 is a block diagram of a clock signal generator and communications apparatus using the clock signal generator according to embodiment 2 of the invention. In Fig. 5, the same reference numerals correspond to those in Fig. 1. Configuration in Fig. 5 differs from that in Fig. 1 in that a clock signal modification terminal 501 is additionally provided and that the clock modification circuit 105 is replaced with a clock signal modification circuit 502. The clock signal modification circuit 502 generates the baud rate control clock signal S502 by masking the rising edge of the original clock signal S102 when the counter value S104 has reached a clock signal modification value S502.

[0031] Fig. 6 shows the operation of the clock signal generator and the communications apparatus using the clock signal generator. Assume that 10 is input as a preset counter value S101 and 4 and 9 are input as clock signal modification values S501. The clock signal modification circuit 502 masks the original clock signal S102 in the case of counter values 4 and 9 and generates the baud rate control clock signal S502. The input circuit 107 sequentially captures input data S106 every three cycles of the rising edge of the baud rate control clock sig-

nal S502, then outputs the captured data as output data S107.

[0032] In this embodiment, a baud rate is realized via accuracy of the baud rate clock signal alone by generating an intermittent baud rate clock signal from a clock generator circuit, instead of using a 9/11 time clock signal.

[0033] As mentioned earlier, an existing clock signal generator circuit is used to generate a baud rate clock signal thus reducing the number of man-hours required for customizing a clock signal generator circuit. Interval of intermittence of a clock signal is externally input so that the baud rate compensation range can be substantially extended, compared with the case in embodiment 1.

(Embodiment 3)

[0034] A clock signal generator and communications apparatus using the clock signal generator according to embodiment 3 of the invention modulates a clock signal output by an existing clock generator circuit in generating a clock signal for controlling the baud rate.

[0035] Fig. 7 is a block diagram of the clock signal generator and the communications apparatus using the clock signal generator according to embodiment 3 of the invention. In Fig. 7, communications apparatus 700 comprises a frequency division value input terminal 701, a modulation indication value input terminal 702, and a modulation circuit 703. The remaining sections correspond to those having the same signs in embodiment 1.

[0036] Fig. 8 is a timing chart explaining the operation of the clock signal generator and the communications apparatus using the clock signal generator shown in Fig. 7. The frequency division circuit divides the frequency of an original clock signal S102 generated in the clock signal generator circuit 102 based on the frequency division value S701. The modulation circuit 703, on obtaining the modulation indication value S702, for example information (frequency, degree of modulation)=(3, 1), outputs a baud rate clock signal whose signal cycles are incremented by one once in three times, as shown in Fig. 8. The input circuit 107 captures input data S106 via the baud rate clock signal S703.

[0037] While the modulation indication value is (frequency, degree of modulation) in embodiment 3, the invention is not limited to this but either or both of the frequency and the degree of modulation may be limited to a predetermined amount and external input may not be required. The degree of modulation can be realized via the falling edge or plus or minus level of a reference clock signal, or via another clock signal.

[0038] While communications apparatus in embodiments 1 through 3 assumes reception only, communications apparatus that performs transmission and reception may be implemented. The same advantage is obtained in case the clock signal frequency of the reference clock signal and that of a clock signal for controlling the baud rate are known, even when both signals are not synchronized.

[0039] As mentioned earlier, a clock signal generator and communications apparatus using the clock signal generator according to the invention has a configuration where an intermittent clock signal having a desired frequency is obtained by adding a peripheral circuit to an existing clock signal generator. This eliminates the need for designing a dedicated clock signal generator for generating a frequency required per communications apparatus, thus reducing the number of man-hours required for design of communications apparatus.

Claims

1. A clock signal generator characterized by comprising

   clock signal generating means for generating a first clock signal,
   counting means for counting the number of clocks of said first clock signal, and
   masking means for generating a second clock signal by masking said first clock signal in case said counting means has reached a preset value.

2. A clock signal generator according to claim 1, characterized in that said counting means is periodically reset and that said masking means has a plurality of values as preset values.

3. A clock signal generator, characterized by comprising a clock signal generating means for generating a first clock signal and
   a modulation means for generating a second clock signal by modulating said first clock signal.

4. Communications apparatus, characterized by using a clock signal generator comprising

   clock signal generating means for generating a first clock signal,
   counting means for counting the number of clocks of said first clock signal, and
   masking means for generating a second clock signal by masking said first clock signal in case said counting means has reached a preset value, to perform data input/output via said second clock signal generated by said clock signal generator.

5. Communications apparatus according to claim 4, characterized in that said counting means is periodically reset and that said masking means has a plurality of values as preset values.

6. Communications apparatus characterized by using a clock signal generator comprising

a clock signal generating means for generating a first clock signal and
a modulation means for generating a second clock signal by modulating said first clock signal, to perform data input/output via said second clock signal generated by said clock signal generator.

Fig. 1

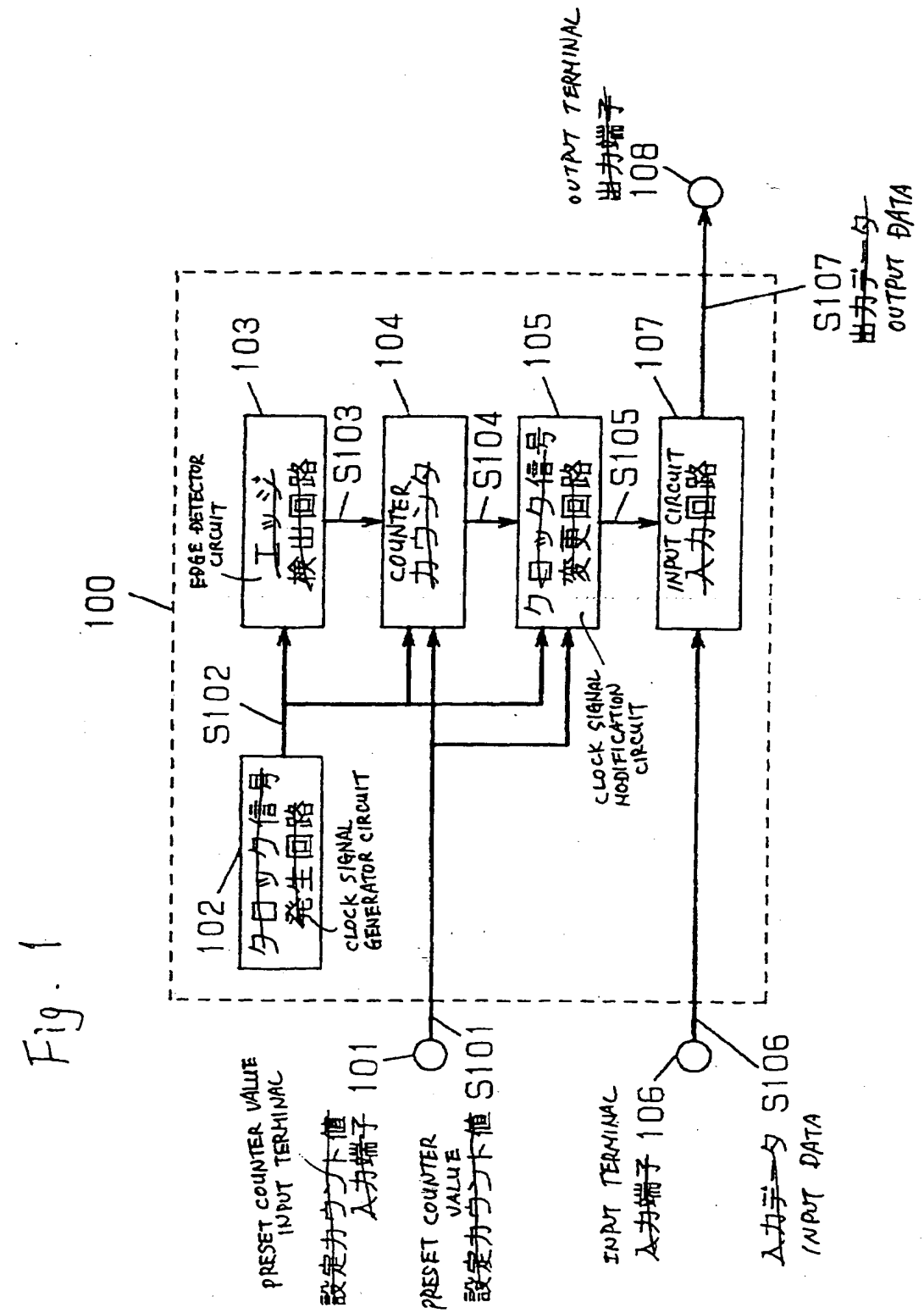


Fig. 2

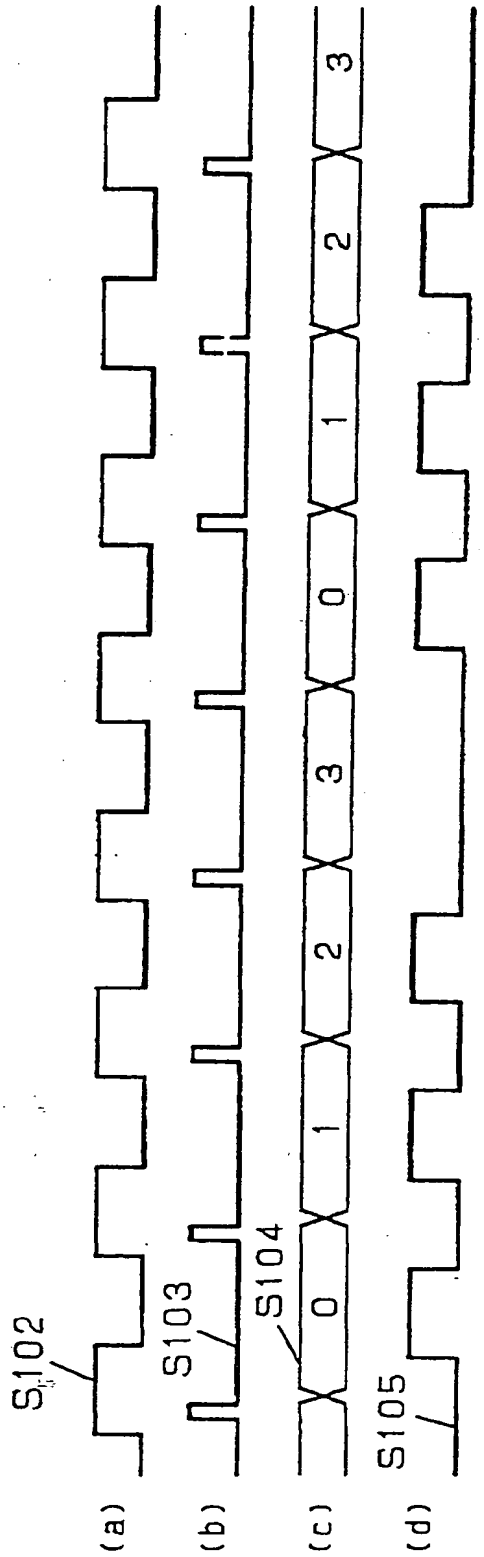
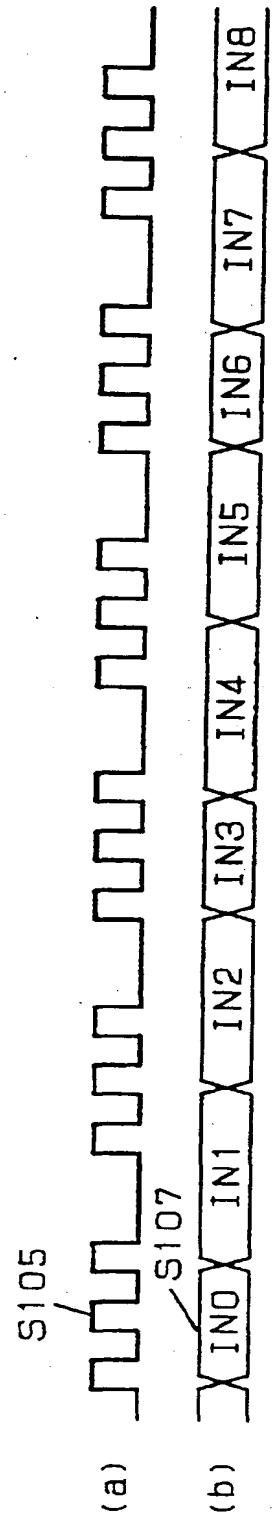


Fig. 3



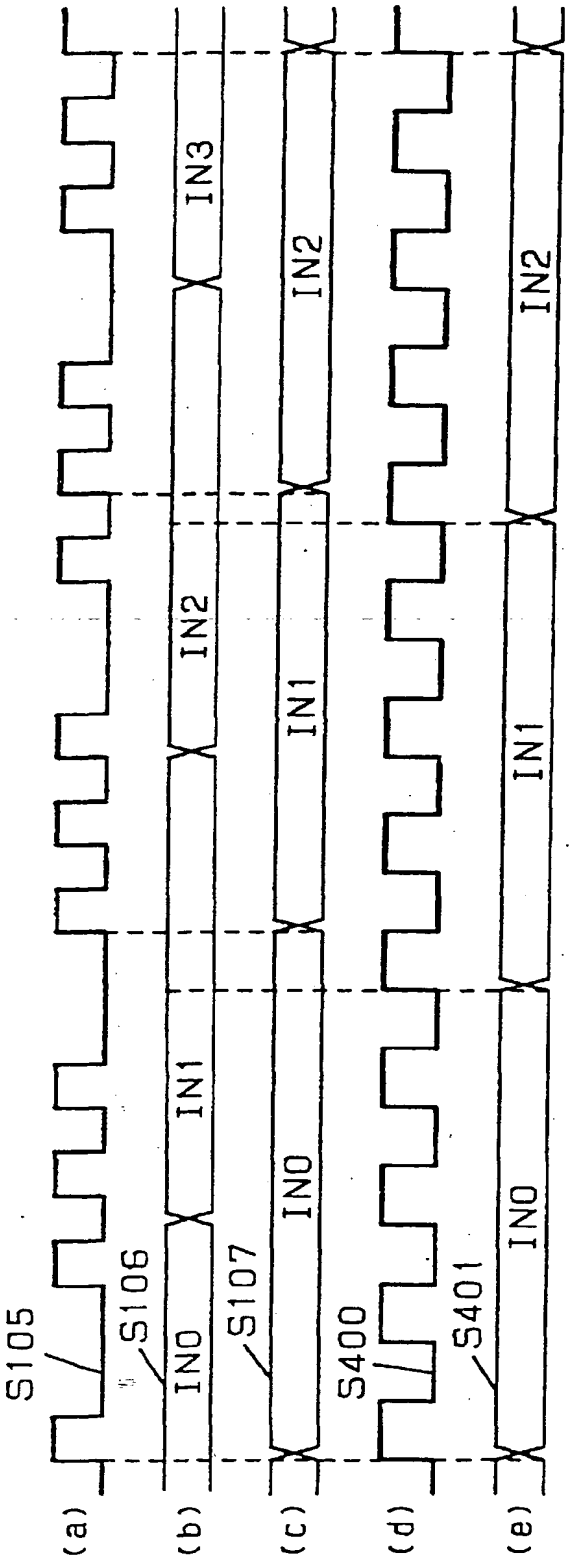


Fig. 4

Fig. 5

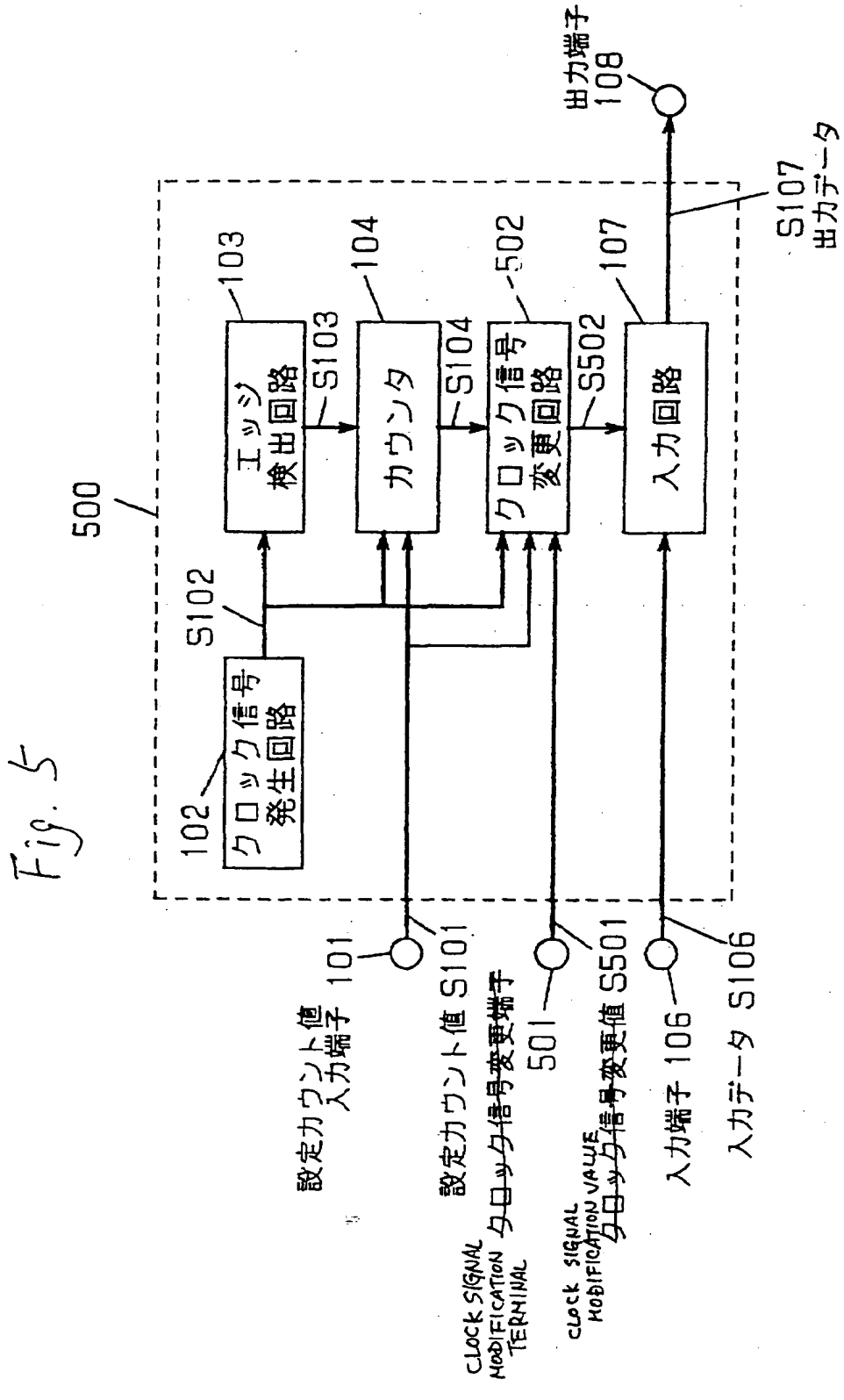


Fig. 6

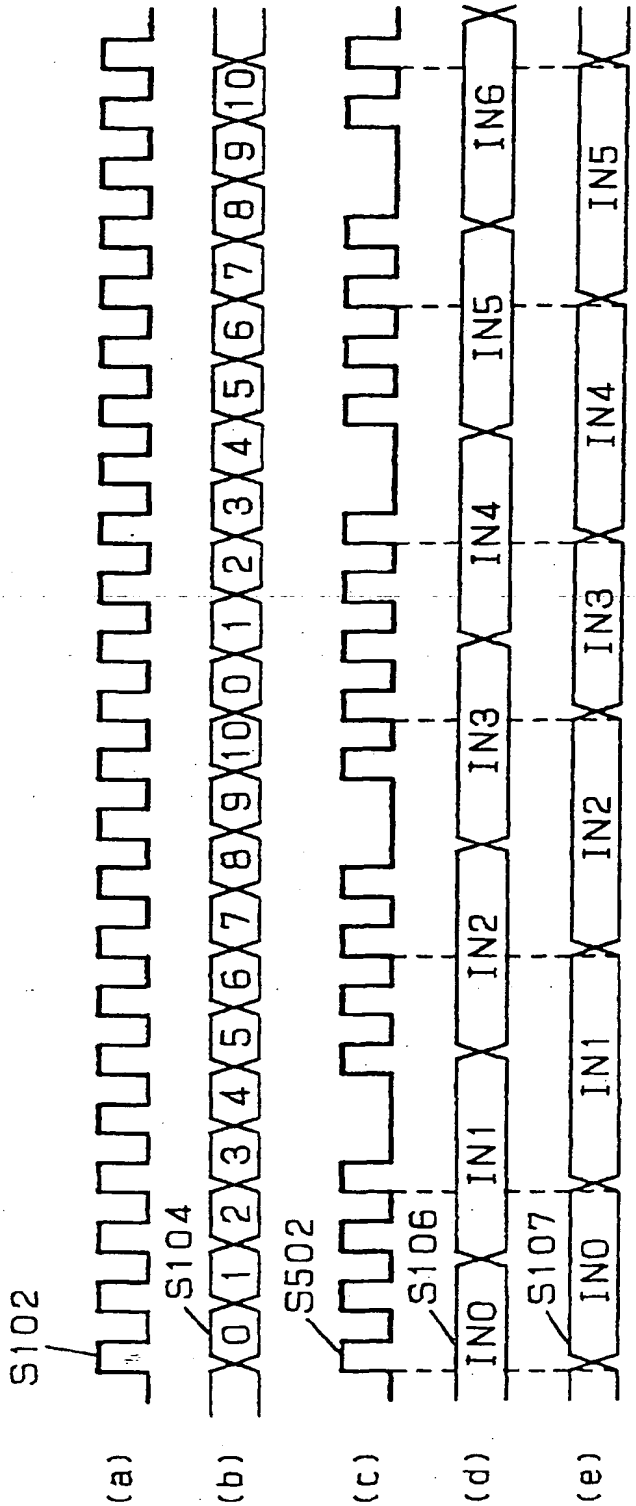
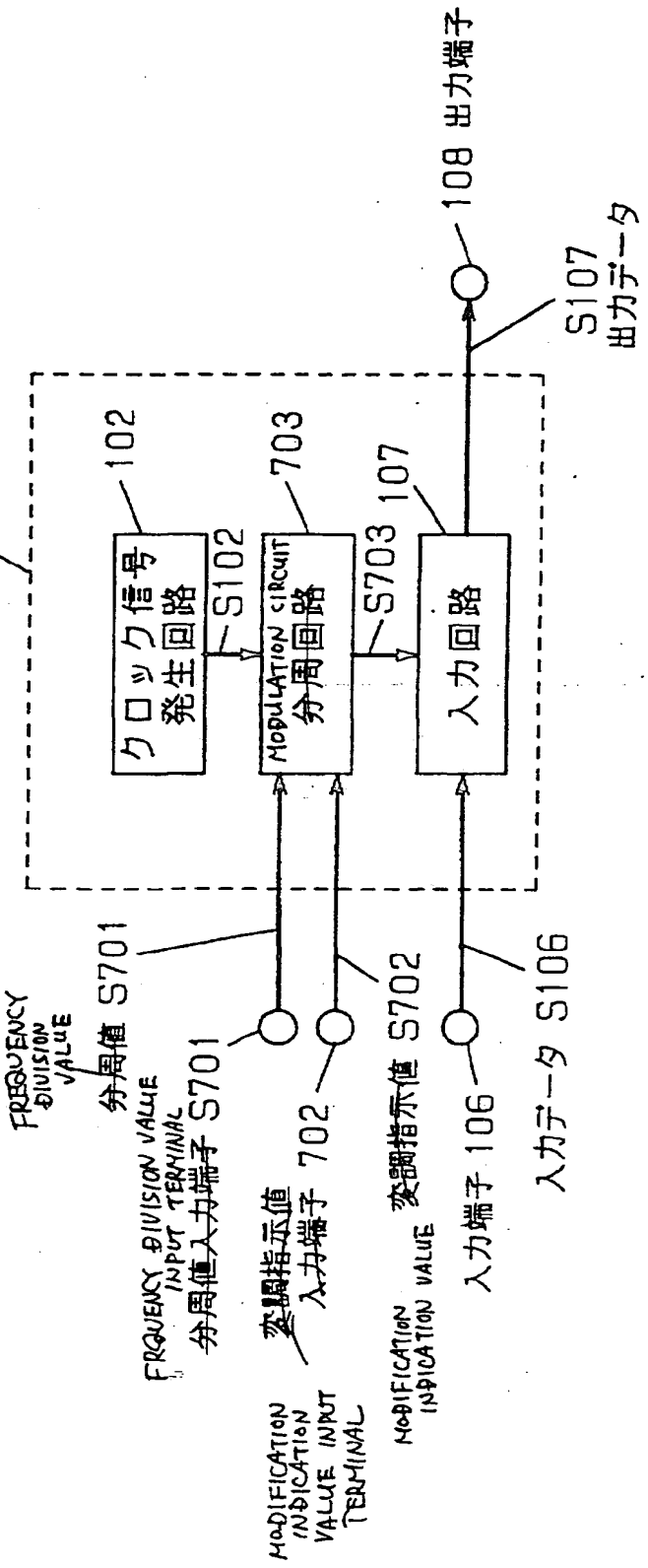


Fig. 7



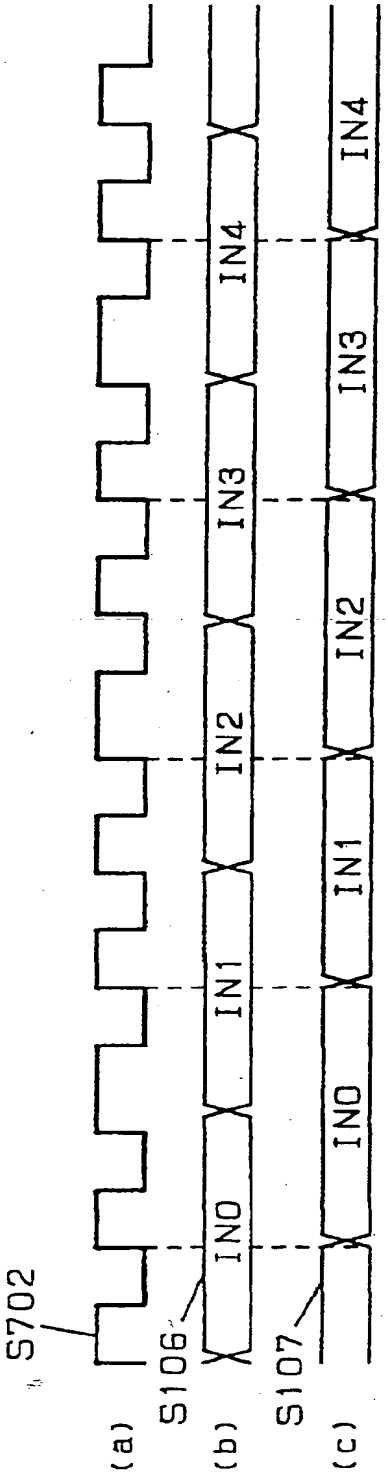


Fig. 8

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 126 618 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
17.10.2001 Bulletin 2001/42

(43) Date of publication A2:
22.08.2001 Bulletin 2001/34

(21) Application number: **01103754.6**

(22) Date of filing: **15.02.2001**

(51) Int Cl.7: **H03L 7/099**, H03K 5/156

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **17.02.2000 JP 2000039510**

(71) Applicant: **MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.**
Kadoma-shi, Osaka-fu 571 (JP)

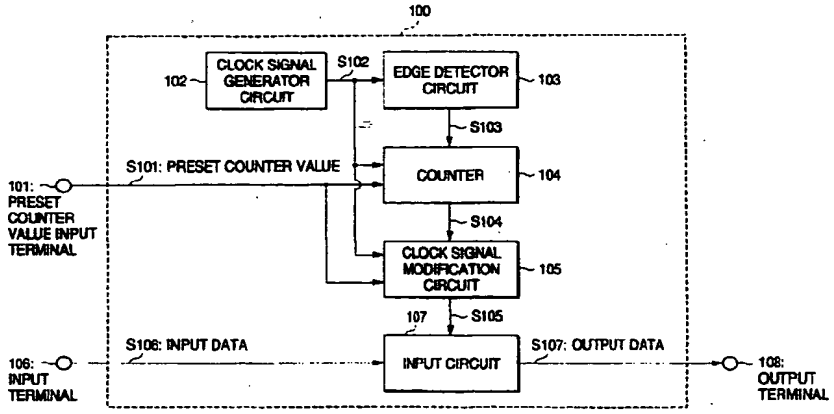
(72) Inventors:
- **Nishio, Takatoshi**
  Hirakata-shi, Osaka (JP)
- **Tabira, Yoshihiro**
  Osaka-shi, Osaka (JP)
- **Kau, Stefan,**
  55411 Bingen (DE)
- **Kiefner, Marcus**
  64297 Darmstadt (DE)

(74) Representative: **Grünecker, Kinkeldey,**
Stockmair & Schwanhäusser Anwaltssozietät
Maximilianstrasse 58
80538 München (DE)

(54) Clock signal generator and communication device using the same

(57) An edge detector circuit 103 detects the edge of an original clock signal S102 generated by the clock signal generator circuit 102. A counter 104 counts the number of edges of the original clock signal S102. The counter 104 is reset when the preset counter value S101 is reached, and repeats counting operation. A clock signal modification circuit 105 masks the original clock signal S102 when the counter value has reached the preset counter value to generate a baud rate control clock signal S105. An input circuit 107 latches input data S106 per predetermined rising edge of the clock signal with the band rate control clock signal S105 and outputs an output signal S107.

FIG. 1



EP 1 126 618 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 01 10 3754

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X Y	US 4 807 156 A (PARISI MICHAEL A) 21 February 1989 (1989-02-21) * figure 4 *	1,2 4,5	H03L7/099 H03K5/156
X Y	US 5 578 968 A (MORI SHINSAKU ET AL) 26 November 1996 (1996-11-26) * figures 2,4 *	1,2 4,5	
Y	U.TIETZE, CH. SCHENK: "Halbleiterschaltungstechnik - Fünfte, überarbeitete Auflage" 1980 , SPRINGER VERLAG , BERLIN HEIDELBERG NEW YORK XP002168817 * page 572 - page 580 *	4,5	
A	EP 0 630 129 A (SEL ALCATEL AG) 21 December 1994 (1994-12-21) * the whole document *	1,2,4,5	
X Y	BUNDGARD T: "BUILD A CYCLE-STEALING RATIO DIVIDER" ELECTRONIC DESIGN,PENTON PUBLISHING, CLEVELAND, OH,US, vol. 47, no. 11, 31 May 1999 (1999-05-31), pages 72-73, XP000912414 ISSN: 0013-4872 * the whole document *	1,2 4,5	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H03L H03K

~~The present search report has been drawn up for all claims~~

Place of search	Date of completion of the search	Examiner
MUNICH	6 June 2001	Oloff, H

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

LACK OF UNITY OF INVENTION
SHEET B

Application Number
EP 01 10 3754

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: 1,2,4,5

   Clock signal generator which uses cycle stealing

2. Claims: 3,6

   A clock signal generator of arbitrary design being used in a data communication device

Cycle-stealing is well known for the generation of "unusal" division ratios - see XP-000912414. The use of clock signal generators with adjustable division ratios for digital data transmission is textbook knowledge - see U. Tietze and Ch. Schenk, Halbleiterschaltungstechnik, Springer Verlag Berlin Heidelberg New York, 5th edition, paragraph bridging pages 578 and 579. A single unifying concept cannot therefore be identified in the present set of claims.

DOCID: <EP___1126618A3_I_>

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 01 10 3754

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

06-06-2001

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4807156 A	21-02-1989	JP 63249659 A	17-10-1988
US 5578968 A	26-11-1996	JP 6132820 A	13-05-1994
		EP 0563400 A	06-10-1993
		WO 9308645 A	29-04-1993
EP 0630129 A	21-12-1994	DE 4319066 A	15-12-1994
		AU 6339694 A	15-12-1994
		CN 1137197 A	04-12-1996
		JP 7143000 A	02-06-1995
		AU 6339594 A	15-12-1994
		CA 2125441 A	10-12-1994
		US 5708687 A	13-01-1998
		US 5790614 A	04-08-1998

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82